Applications of Custom VLSI Circuits in Exploration Seismology

Rick Ottolini and John Newkirk

Abstract

Custom *V*ery *L*arge *S*cale *I*ntegrated circuits can be used to increase the speed, portability, reliability, and economy of computations in exploration seismology. Better design tools have made custom VLSI circuits accessible to non-engineers and more economical for everyone. Applications to exploration seismology include specialized data displays, custom array processors, and electronics to do computation at the data's source. This paper presents a case history of a high speed (250 kilohertz) deconvolution filter implemented with custom VLSI.

Introduction

The capabilities of integrated circuits have been increasing at a tremendous rate for the past 25 years. Starting with simple circuits with only a few transistors, todays state-of-the-art microprocessors have nearly 500,000 transistors (see Figure 1). That is as complex as the mainframes of only a few years ago. Such capability can be used to build complex computers and dense memories, products with large markets. It can also be used to build special-purpose systems that are significantly superior to systems built with standard components.

Unfortunately, with the tremendous increase in capability has come an alarming increase in the cost of doing a design. A complex chip now typically requires dozens of man years of design time. Thus, only designs that would lead to large production runs have been considered feasible.

Recent research breakthroughs have dramatically reduced the cost of designing these custom circuits, often by a factor of ten and sometimes by much more. This research, done

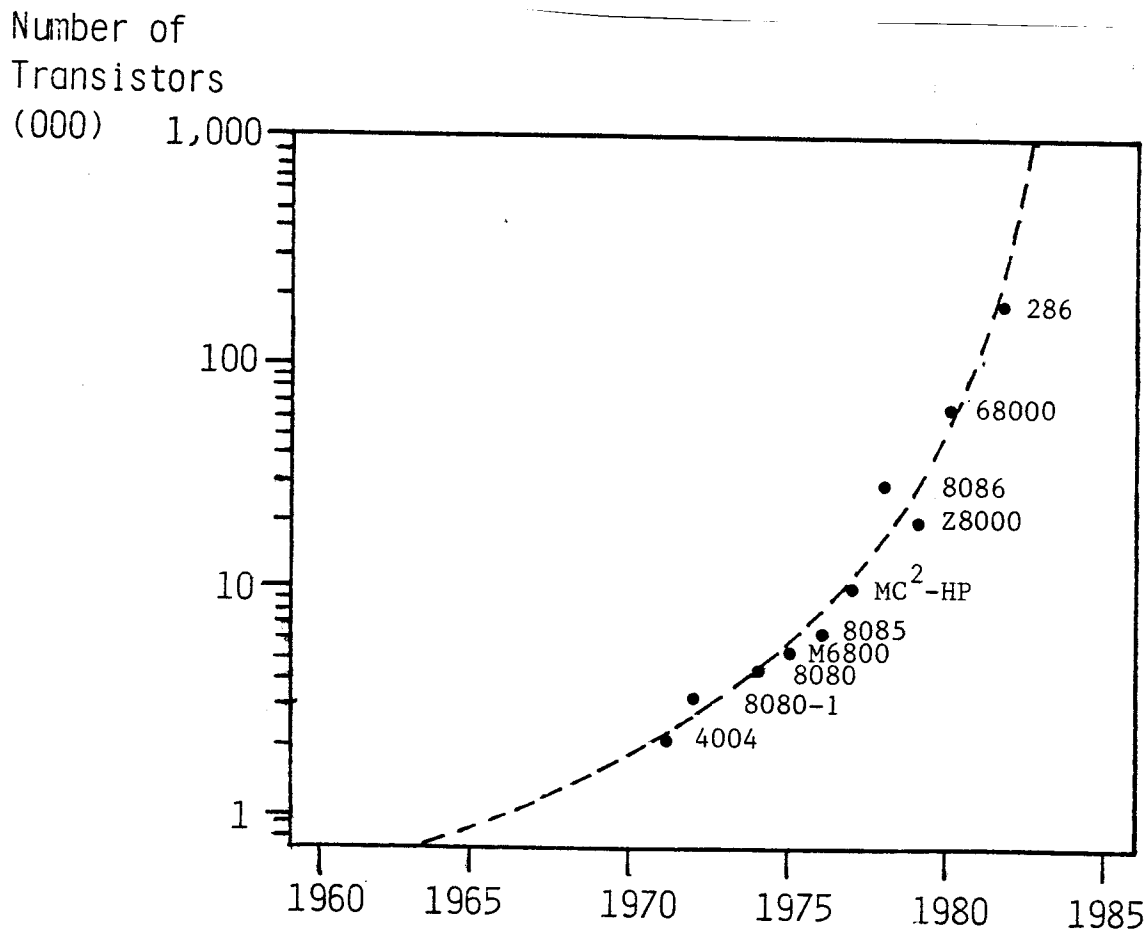

FIG. 1. The growth of microcomputer complexity with time.

primarily at Stanford and a few other universities, has focused on simplifying the design process and greatly increasing the use of automation.

Increased Accessibility

Designing a VLSI circuit is not much different from writing a computer program. Design aids, sometimes refered to as a *silicon compiler*, translate high-level descriptions of computational mechanisms into the low-level descriptions necessary for manufacturing a VLSI circuit. Such a compiler is similar to its software analog; it includes a library of

predefined elements, debugging simulators, powerful verification tools, as well as tools such as routing and testing support software.

Almost any person who has written computer programs can learn to use these design aids after a few weeks of training. Just as high-level computer languages make it unnecessary for a programmer to be concerned with the details of how the computer works, so do the design tools make many of the details of chip design nearly transparent to the circuit designer. The case study presented in this paper was designed by a geophysicist who had only a month's training and who had never designed an integrated circuit before. The experience at Stanford clearly shows that for such custom applications, the ideal team is not the traditional group of two dozen specialists. Instead, it is a scientist in the field of computational interest with some training in chip design and an engineering specialist in VLSI design.

At Stanford, over 200 such chips have been fabricated over the past 4 years; the current design laboratory has students designing 10,000 transistor systems in 10 weeks (an 8080 microprocessor is only 3,000 transistors). Most of these students have an electrical engineering background, but many are from computer science, chemistry, geophysics, and even the business school.

Most students subsequently test their projects. Unfortunately, for some students, 10 weeks is too short a time to get everything done. However, for those projects that were thoroughly checked before they were fabricated, nearly all of them work.

Motivation

Reducing a digital system to a minimum number of chips (often one), by using custom integrated circuits, can have a dramatic effect in a large number of ways. The reliability and cost of computation hardware is proportional to the number of physical packages in the computing system. Since custom VLSI circuits reduce this count to a minimum, thereby maximizing reliability and minimizing cost. (Even in low volumes, custom ICs can be manufactured for 10 to 20 dollars.) Having an entire system on a 1/4" square of glass also reduces the size and power requirements for the unit, a valuable asset in the field.

Custom VLSI also increases the *speed* of computation, often by several orders of magnitude over a general purpose or array processor, for several reasons. On-chip, signals propagate very quickly; the transit time for most transistors is less than a nanosecond! Also, with custom hardware, the overhead of interpreting software computation commands is eliminated or greatly reduced. Computation can also be distributed among many identical VLSI circuits (whether on the same chip package or in several chip packages) to increase

the speed of computation. This is a very powerful idea, because the economics of VLSI circuits is that most of the cost is in designing and manufacturing that first circuit. Subsequent copies are essentially free.

Finally, the flexibility offered to the designer of custom ICs often leads to new applications never foreseen in older technologies. For example, the advent of the pocket calculator was only possible after ICs had enough capability.

Exploration Seismology Applications

Computation at the Data Source

Some computation can be done right at the data source itself. This reduces the cost and needs for communications and centralized computing. Data can be *digitized* directly at the geophone to prevent transmission noise. Some source waveform and reverberations can be *deconvolved* at the geophone. Multiple source excitations could be digitally *stacked* at the receiver point. Receiver *array summation* time shifts and weights could be modified under dynamic control. VLSI circuits could attach routing and bookkeeping information to the data. The cost of circuit design and manufacture would be easily absorbed over thousands of geophones.

Custom Array Processors

After as much computing as is reasonable has been done in the field, custom VLSI circuits can be used for processing the consolidated data. There are many processing algorithms (gain, moveout, deconvolution, correlation) that work on local pieces of the data, usually single traces. Such algorithms can easily exploit the parallelism that VLSI computing devices offer. Furthermore, many global computations (FFT's, difference calculations) can be decomposed into distributed, parallel computations. Once a VLSI floating point computing element has been built, copies of it are almost free.

Data Display

At all stages of processing and interpretation it is important to see a display of the data. Considerable computation is necessary to access selected data and convert them into patterns of ink or light. High performance, custom VLSI circuits can assist innovative graphical techniques such as real time display, interactive graphics, and animation.

Case History of A Deconvolution Chip

The design in Figures 2 and 3 is a high speed deconvolution filter circuit which could be placed within individual geophones. The circuit of Figure 3 implements the general finite impulse response filter of Figure 2. The filter works in two phases. First, the filter coefficients are pre-loaded into the circuit memory. Then data samples are multiplied by their coefficients and added to the accumulating results.

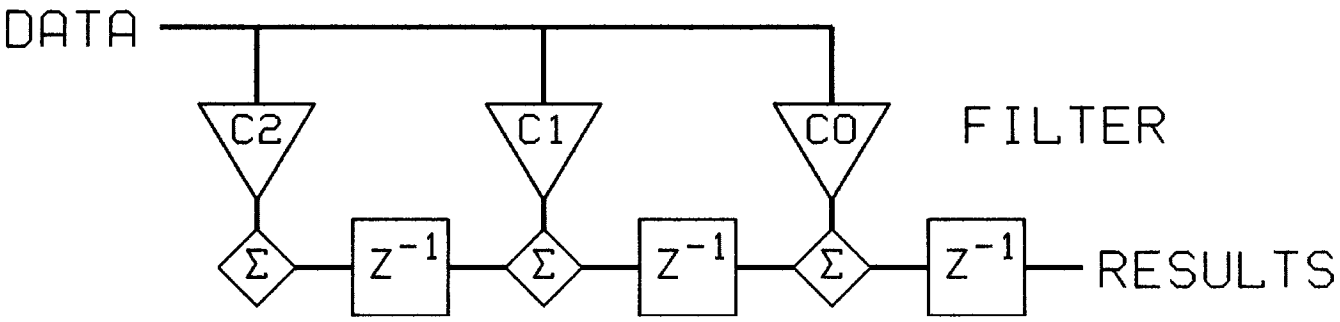

FIG. 2. Convolution algorithm embodied in the VLSI circuit of Figure 3. Triangles represent scaling factors, diamonds represent summation, and squares represent unit delay. The algorithm is modular and may easily be expanded to an arbitrary number of filter coefficients.

The convolution is very fast because a multiplier-adder unit is replicated for every filter point. In this way, results are output as fast is data is input, which is about 200 nanoseconds per data sample. Given that the multiplication rate is competitive with current array processors, then this circuit will be a hundred times faster than an array processor for a filter one hundred points long (and on each geophone too!).

The basic circuit in Figure 3 contains forty cells. Each cell has a 1 bit multiplier-adder, one bit of filter memory, and one bit of accumulator memory. Stacking up cells into a column yields an eight-bit filter coefficient, an eight-bit accumulator, and an eight-bit serial multiplier. There are five filter coefficients, or rows, in this figure. The precision can be increased by making the columns taller and filter coefficients can be added by increasing the number of columns. Also, chips can be interconnected sideways to increase the number of filter coefficients.

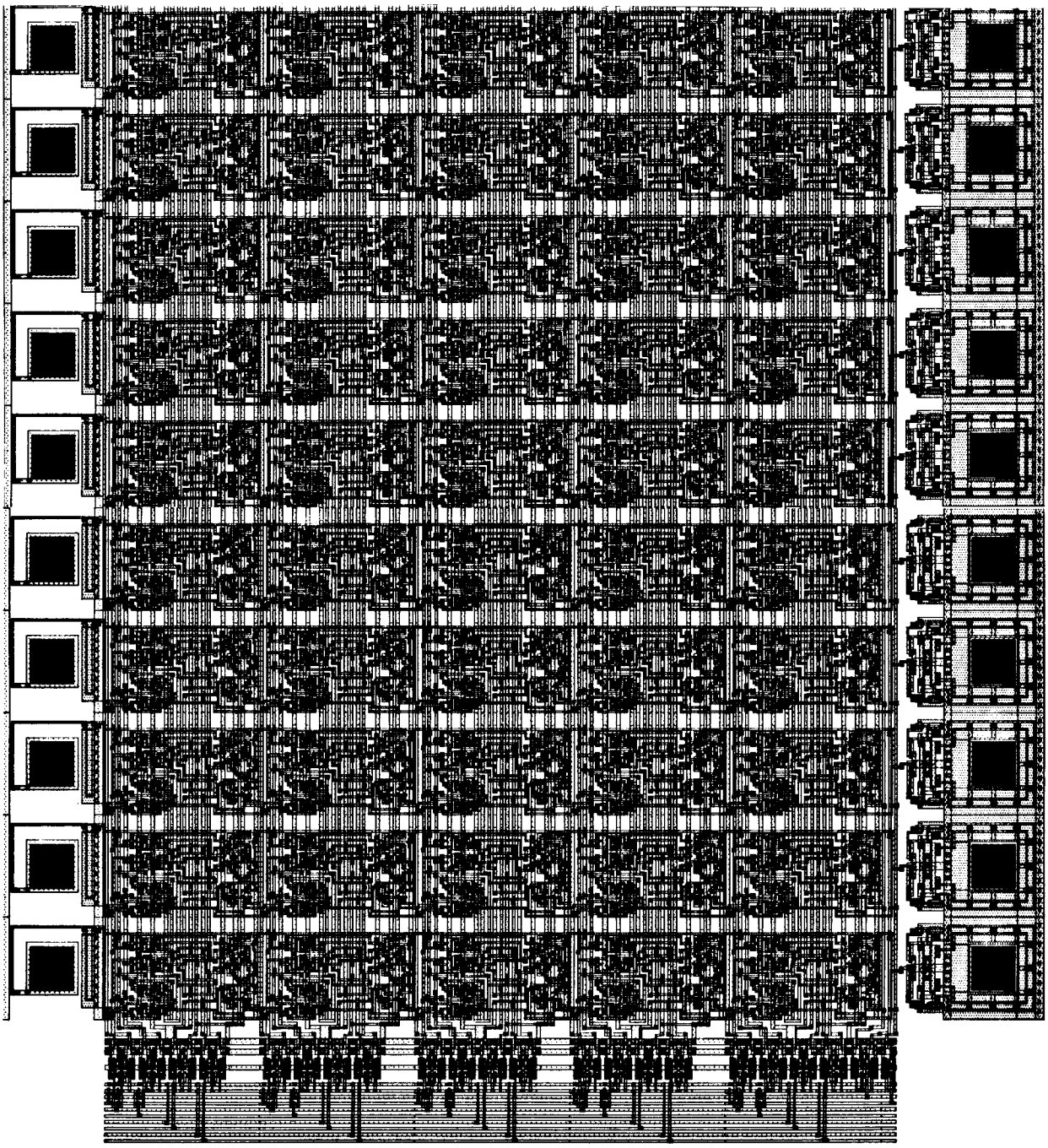

FIG. 3. Composite mask of the VLSI circuit described in the text and Figure 2.

At the base of the chip is the multiplier control bus and control for moving the filter coefficients and results through memory. Not shown is a finite state machine (built for a programmed logic array) for generating the control signals for a complete multiplication cycle.

This architecture exhibits several important properties in good VLSI circuit design. It is *modular*, most of the capability being concentrated in a few basic cells. The computational power of the circuit is increased by *replication* of the basic cell. The circuit obtains high speed through a large amount of *parallel computation* as a result of by the modular design. Control, data, and power wires are cleverly arranged within the basic cell so as to virtually eliminate the complex wiring commonly seen in VLSI layouts.

This chip took three weeks to design in 1980 for an electrical engineer and geophysicist (both VLSI neophytes). The software design tools were provided by the Stanford VLSI Project running on an UNIX VAX in the department of electrical engineering. A subset of this chip (five cells and the finite state machine) was fabricated in 5 micrometer NMOS technology. As part of a 100 project, 5 chip wafer fabrication run sponsored by Xerox Palo Alto Research Center, the chip cost was $500 and turn-around time was a month. Limited testing showed that most of the circuit performed as designed, except for a polarity reversal in the multiplier-adder.

It must be admitted that this particular circuit design is not the best implementation for an exploration seismology deconvolution chip. The circuit designers were focusing on elegance and performance in this training exercise rather than a purely commercial implementation. For one thing the circuit runs about a thousand times faster than is necessary for one millisecond sample rate deconvolution in exploration seismology. Sacrificing speed by going to a less parallel computational design would free some chip real estate for storing more filter coefficients or incorporating more computation functions. Nevertheless, this design illustrates the power of this new technology for solving geophysical data processing problems.

Acknowledgments

Rex Heller, Stanford 1980 E.E. M.S., helped design this circuit. The VLSI circuit design laboratory is run by Rob Mathews and John Newkirk, electrical engineering assistant professors at Stanford.

Further Information

If the reader wants further information on VLSI technology or has suggestions for VLSI circuit applications in exploration seismology, please contact Professor John Newkirk in the electrical engineering department at Stanford.

General Reference

Mead, C. and Conway, L., 1980, Introduction to VLSI Systems, Addison-Wesley